

MULTIMEDIA



UNIVERSITY

STUDENT ID NO

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# MULTIMEDIA UNIVERSITY

## FINAL EXAMINATION

TRIMESTER 1, 2015/2016

### ECP2216 – MICROCONTROLLER AND MICROPROCESSOR SYSTEMS ( All sections / Groups )

16 OCTOBER 2015  
9.00 a.m – 11.00 a.m  
( 2 Hours )

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#### INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 11 pages with 5 Questions only.
2. Attempt **ALL FIVE COMPULSORY** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

**Question 1**

- (a) List out any **TWO** differences between microcontrollers and microprocessors.  
[2 marks]
- (b) A 32-bit microcontroller is designed to access a 4GB memory.  
What is the size of the address bus in this microcontroller system?  
*(You are required to show out all working steps)* [3 marks]

- (c) Given an 8-bit binary number, X, as below:

$$X = 10101000_2$$

Convert X into decimal number, if:

- (i) X is an unsigned number. [2 marks]  
(ii) X is a signed number. [3 marks]  
*(You are required to show out all working steps)*
- (d) (i) List out **THREE** shortcomings of using four coupled single-core processor systems as compared to Quad-core processor systems.  
[6 marks]
- (ii) Illustrate by sketching the implementation of Quad-core processor systems and four coupled single-core processor systems.  
[2 marks]
- (iii) 80386DX Intel 32-bit microprocessor has six functional units. Name any **ONE** of these functional units and briefly explain its purpose.  
[2 marks]

Continued .....

**Question 2**

- (a) Identify the byte address and bit position involved in the following instruction:

SETB 26

[2 marks]

- (b) (i) Identify which I/O port of 8051 microcontroller is used for address/data multiplexing during external memory access.

[1 mark]

- (ii) Explain the term “*address/data multiplexing*” which is used in 8051 microcontroller.

[1 mark]

- (c)

MOV R3, #78H

MOV A, #0A8H

ADD A, R3

Consider the above assembly language instruction sequence. Identify the contents of Program Status Word (PSW) and Accumulator (A) after the execution of this instruction sequence. (*Assume initial value: A=00H and PSW=00H*)

[3 marks]

- (d) An 8051 microcontroller based system is designed to address contiguous 16Kbytes of external memory space. 12Kbytes of external data memory should occupy the first portion of the memory space followed by 4Kbytes of external program memory. Available memory ICs are 4Kbytes ROM and 4Kbytes RAM.

(i) Identify the number of ROM ICs and RAM ICs required. [1 mark]

(ii) Calculate the size of address bus required. [2 marks]

- (iii) Draw and label the system configuration showing the 8051 signal lines to be used for data, address and control buses.

[10 marks]

Continued .....

**Question 3**

- (a) Table Q3(a) shows the initial contents of on-chip RAM locations and registers in 8051 microcontroller.

Address	Content	Register	Content
30H	00H	ACC	FFH
45H	ABH	B	08H
58H	02H	SP	07H
ECH	03H	R0	12H
EDH	04H	R1	ECH

*Table Q3(a)*

Consider the following MCS-51 instruction sequence.

```

ANL A, 30H
INC R1
MOV SP, #2FH
MOV 45H, A
MOV A, R1
MOV R0, A
ADD A, @R1
PUSH 58H

```

- (i) Determine the addressing mode used for the destination and source operands in each instruction.

[5 marks]

- (ii) Determine the final contents of each on-chip RAM location and register after the execution of the instruction sequence. (*Hints: You may use Table Q3(b) to assist you.*)

Address	Final Content	Register	Final Content
30H		ACC	
45H		B	
58H		SP	
ECH		R0	
EDH		R1	

*Table Q3(b)*

[8 marks]

Continued .....

- (b) Find the corresponding MCS-51 assembly language instructions for the sequence of machines codes as shown in Table Q3(c).

Address	Machine Codes
0008H	75H 4FH A0H
000BH	A9H 4FH
000DH	D9H FEH
000FH	22H

Table Q3(c)

[5 marks]

- (c) Consider the following MCS-51 assembly language subroutine.

```
DELAY: MOV R0, #250
REPEAT: NOP
        NOP
DJNZ R0, REPEAT
RET
```

Assume 12 MHz crystal frequency is used, calculate the total execution time of the subroutine.

[2 marks]

Continued .....

#### Question 4

- (a) An 8051 microcontroller system is to be designed to generate two waveforms at Port 2 pin 2 and Port 2 pin 3. Figure 4(a) shows INT1 pin and INT0 pin connected to a switch that is normally high. Whenever INT1 pin goes low, it generates waveform 1 using timer 1 interrupt. Whenever INT0 pin goes low, it generates waveform 2 using timer 0 interrupt.

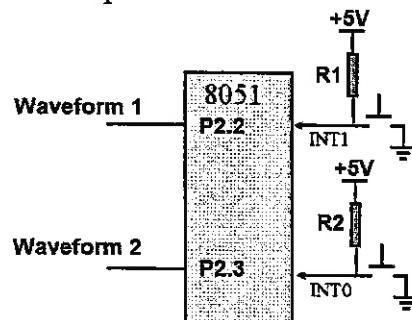


Figure 4(a)

The specification of both waveforms are given as below:

*Waveform 1: Pulse Train with frequency of 1 KHz.*

*Waveform 2: Pulse Train with frequency of 2 KHz.*

Write a MCS-51 assembly language program to perform the task.

[10 marks]

- (b) Interrupt is one of the most essential and powerful features in microcontroller. It is an event that momentarily interrupts the main program, hands over the control to a service routine, performs the event-related task and continues the main program flow where it had left off. *List ALL interrupts sources which are available in 8051 microcontroller and arrange them in the order corresponding to their default priority.*

[5 marks ]

- (c) Consider an 8051 microcontroller operates at 11.0592MHz crystal frequency and needs to be initialized as an 8-bit UART at 2400 baud rate generated by Timer 1.

- (i) Determine the values of SCON register and TMOD register to be initialized.

[2 marks]

- (ii) Compute the required reload value for Timer 1 register.

*Assume SMOD is cleared.*

[3 marks]

Continued .....

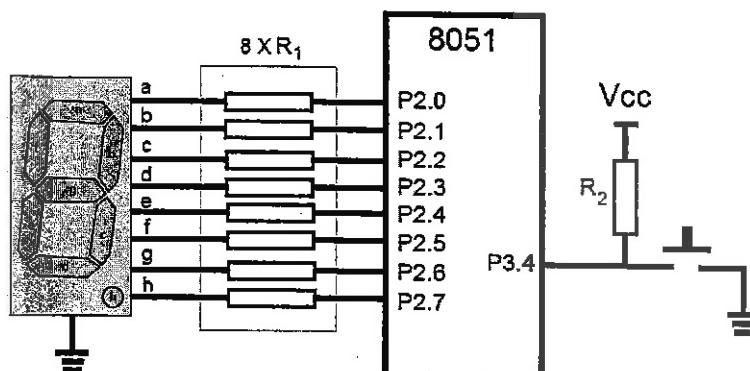
### Question 5

- (a) Table 5(a) shows the bit patterns for each character to decode the seven-segment display.

**Table 5(a)**

<i>Digit</i>	<i>h</i>	<i>g</i>	<i>f</i>	<i>e</i>	<i>d</i>	<i>c</i>	<i>b</i>	<i>a</i>
E	0	1	1	1	1	0	0	1
C	0	0	1	1	1	0	0	1
P	0	1	1	1	0	0	1	1
2	0	1	0	1	1	0	1	1
1	0	0	0	0	0	1	1	0
6	0	1	1	1	1	1	0	1

Figure 5(a) shows an 8051 microcontroller system with Port 2 interfaces to a seven-segment display device and P3.4 interfaces to a press button.



**Figure 5(a)**

Write a MCS-51 assembly language subroutine called **7SEGMENT** to perform the following process.

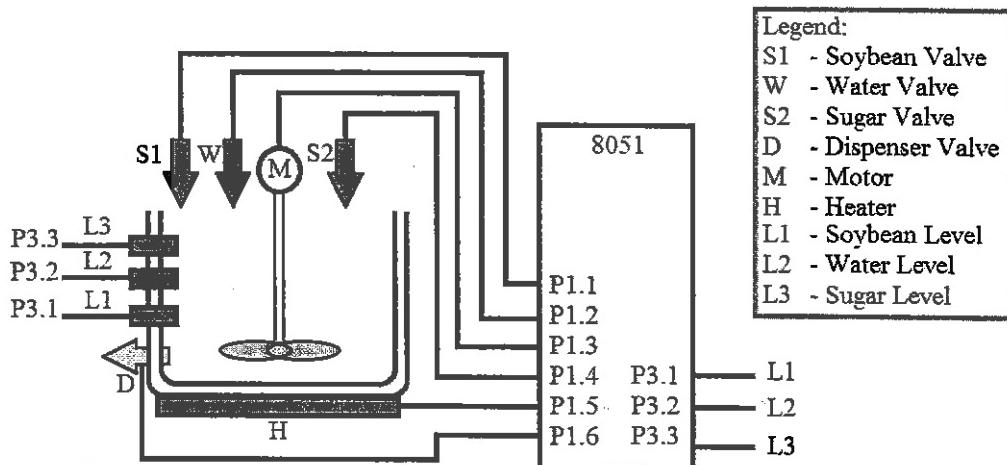
1. Wait for the button press on P3.4.
2. Once the button is pressed, seven-segment display will start to show the characters in sequence starting from E, C, P, 2, 2, 1 and 6 with time interval between each character is 0.5 second.
3. Then, return from subroutine.

*NOTE: Assume 1 second delay subroutine **DLY0\_5S** is available.*

[10 marks]

Continued .....

- (b) Automatic soymilk maker commonly use blending machine to blend soybean and heater to cook soymilk. An 8051 microcontroller based automatic soymilk maker is shown in Figure 5(b) which performs the following process:



**Figure 5(b)**

- i. Initially, all valves, heater and motor are closed.
- ii. The mug is first filled with soybean through a solenoid Valve S1.
- iii. When the soybean reaches Level L1, Valve S1 is closed and the mug is now filled with drinking water via Valve W.
- iv. When the mixture in the mug reaches Level L2, Valve W is closed.
- v. The mug is then filled with sugar through Valve S2.
- vi. When the mixture reaches Level L3, Valve S2 is closed and the blender motor starts the blending process that last for approximately 1 minutes.
- vii. Next, heater starts the cooking process which boils the soymilk for 3 minutes.
- viii. Finally, the dispenser Valve D opens to dispense the cooked soymilk.
- ix. The whole process is completed and stops.

The output lines **P1.1**, **P1.2**, **P1.4** and **P1.6** from 8051 microcontroller provide signals to the solenoid valves. A logical **HIGH** from the lines will open the corresponding valve. The output lines **P1.3** and **P1.5** from 8051 microcontroller provide signals to the blender motor and heater respectively which are both activated by a logical **HIGH**. The mug has three level sensors that send signals to input lines **P3.1** to **P3.3**. A logical **LOW** from the sensor indicates that the level has been reached. Write a MCS-51 assembly language program to carry out the process. Assume 12MHz crystal frequency is used.

[10 marks]

**End of Page**

## APPENDIX

### Special Function Register Formats

#### Interrupt Enable (IE)

Bit Addr.	AFH	-	-	ACH	ABH	AAH	A9H	A8H
Name	EA	-	-	ES	ET1	EX1	ET0	EX0

BIT	SYMBOL	FUNCTION (Enable=1, Disable=0)
IE.7	EA	Global enable/disable. EA = 1, each individual source is enabled/disabled by setting/clearing its enable bit. EA = 0, disable all interrupts.
IE.6	-	Undefined
IE.5	-	Not implemented in 8051. ET2 for 8052.
IE.4	ES	Serial port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt enable bit.

#### Interrupt Priority (IP)

Bit Addr.	-	-	-	BCH	BBH	BAH	B9H	B8H
Name	-	-	-	PS	PT1	PX1	PT0	PX0

BIT	SYMBOL	FUNCTION (Enable=1, Disable=0)
IP.7	-	Undefined
IP.6	-	Undefined
IP.5	-	Not implemented in 8051. PT2 for 8052.
IP.4	PS	Serial port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt priority bit.

#### Interrupt Vectors

Interrupt Source	Flag	Vector Address
System Reset	RST	0000H
External 0	IE0	0003H
Timer 0	TF0	000BH
External 1	IE1	0013H
Timer 1	TF1	001BH
Serial Port	RI & TI	0023H
Timer 2 (8052)	TF2 or EXF2	002BH

**Program Status Word (PSW)**

Bit Addr.	D7H	D6H	D5H	D4H	D3H	D2H	-	D0H
Name	CY	AC	F0	RS1	RS0	OV	-	P

**Serial Control (SCON)**

Bit Addr.	9FH	9EH	9DH	9CH	9BH	9AH	99H	98H
Name	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

BIT	SYMBOL	FUNCTION
SCON.7	SM0	Serial port mode bit 0 (see Table A.1).
SCON.6	SM1	Serial port mode bit 1 (see Table A.1).
SCON.5	SM2	Serial port mode bit 2; enables multiprocessor communications in modes 2 and 3; RI will not be activated if received 9 <sup>th</sup> bit is 0. In mode 1, if SM2 = 1, then RI will be activated only if a valid stop bit was received. In mode 0, SM2 should be 0.
SCON.4	REN	Receiver enable; must be set to receive characters.
SCON.3	TB8	Transmit bit 8; 9 <sup>th</sup> bit transmitted in modes 2 and 3; set/cleared by software.
SCON.2	RB8	Receive bit 8; 9 <sup>th</sup> bit received.
SCON.1	TI	Transmit interrupt flag; set at end of character transmission; cleared by software.
SCON.0	RI	Receive interrupt flag; set at end of character reception; cleared by software.

Table A.1 The 8051 Serial Port Mode Selection

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	Fixed
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fixed
1	1	3	9-bit UART	Variable

**Timer Control (TCON)**

Bit Addr.	8FH	8EH	8DH	8CH	8BH	8AH	89H	88H
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer-1 overflow flag. Set by hardware on overflow. Cleared by hardware when processor vectors to interrupt routine. Must be cleared by software when not involve interrupt.
TCON.6	TR1	Timer-1 run control bit. Set/cleared by software to turn timer/counter on/off.
TCON.5	TF0	Timer-0 overflow flag. Do the same function as TF1 but for Timer-0.
TCON.4	TR0	Timer-0 run control bit. Do the same function as TR1 but for Timer-0.
TCON.3	IE1	External interrupt-1 edge flag. Set by hardware when interrupt-1 falling edge is detected. Cleared by hardware when interrupt is processed.
TCON.2	IT1	Interrupt-1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
TCON.1	IE0	External interrupt-0 edge flag. Do the same function as IE1 but for external interrupt-0.
TCON.0	IT0	Interrupt-0 Type control bit. Do the same function as IT1 but for external interrupt-0.

**Timer Mode (TMOD)**

Bit	7	6	5	4	3	2	1	0
Name	GATE	C/T	M1	M0	GATE	C/T	M1	M0

BIT	SYMBOL	FUNCTION
TMOD.7	GATE1	When this bit is set the timer will only run when INT1 (P3.3) is high (hardware control). When this bit is cleared the timer will run regardless of the state of INT1 (software control).
TMOD.6	C/T1	Timer / Counter select bit. $C / \bar{T} = 0 \rightarrow$ Timer operation. $C / \bar{T} = 1 \rightarrow$ Counter operation.
TMOD.5	M1	Mode selection bits (see Table A.2). [for timer 1]
TMOD.4	M0	Mode selection bits (see Table A.2). [for timer 1]
TMOD.3	GATE0	Exactly the same function as GATE1 but for Timer0
TMOD.2	C/T0	Exactly the same function as C/T1 but for Timer0
TMOD.1	M1	Mode selection bits (see Table A.2). [for timer 0]
TMOD.0	M0	Mode selection bits (see Table A.2). [for timer 0]

Table A.2 Timer Mode Selection

M1	M0	Timer Mode	Description of Mode
0	0	0	13-bit Timer
0	1	1	16-bit Timer
1	0	2	8-bit auto-reload
1	1	3	Split timer mode

## MCS-51 Opcode Map

Instruction Operands Syntax	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 NOP	SE JBC bit, rel 2C	JBS bit, rel 2C	JNC bit, rel 2C	JZ bit, rel 2C	SIMP bit, rel 2C	JNZ bit, rel 2C	JMP (P1) 2C	JMP (P2) 2C	JMP (P3) 2C	JMP (P4) 2C	ORL C, Rn 2C	ANL C, Rn 2C	MOV C, Rn 2C	PUSH di 2C	POP di 2C	MOVX A, @R1 2C
1 AJMP (P0) 2C	ACALL (P1) 2C	ACALL (P2) 2C	ACALL (P3) 2C	ACALL (P4) 2C	ACALL (P5) 2C	ACALL (P6) 2C	ACALL (P7) 2C	ACALL (P8) 2C	ACALL (P9) 2C	ACALL (P10) 2C	AJMP (P1) 2C	ACALL (P11) 2C	ACALL (P12) 2C	ACALL (P13) 2C	ACALL (P14) 2C	ACALL (P15) 2C
2 LJMP #rel 16 2C	LJCALL #rel 16 2C	RET	RLC A 1C	XRL A 1C	XRL A 1C	XRL A 1C	XRL A 1C	XRL A 1C	XRL A 1C	XRL A 1C	ORL C, Rn 2C	ANL C, Rn 2C	MOV C, Rn 2C			
3 RR RRC A 1C	RRC A 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	ADD A, Rn 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
4 INC A 1C	INC A 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	DEC A, Rn 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
5 INC Rn 1C	INC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	DEC Rn 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
6 INC R0 1C	INC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	DEC R0 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
7 INC R1 1C	INC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	DEC R1 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
8 INC R2 1C	INC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	DEC R2 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
9 INC R3 1C	INC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	DEC R3 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
A INC R4 1C	INC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	DEC R4 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
B INC R5 1C	INC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	DEC R5 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
C INC R6 1C	INC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	DEC R6 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
D INC R7 1C	INC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	DEC R7 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
E INC R8 1C	INC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	DEC R8 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C
F INC R9 1C	INC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	DEC R9 1C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C	MOV A, Rn 2C